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High quality factor HTS Josephson junctions on low loss substrates

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Abstract
We have extended the off-axis biepitaxial technique to produce YBCO grain boundary junctions on low loss substrates. Excellent transport properties have been reproducibly found, with remarkable values of the quality factor I_cR_n (with I_c the critical current and R_n the normal state resistance) above 10 mV, far higher than the values commonly reported in the literature for high temperature superconductor (HTS) based Josephson junctions. The outcomes are consistent with a picture of a more uniform grain boundary region along the current path. This work supports a possible implementation of grain boundary junctions for various applications including terahertz sensors and HTS quantum circuits in the presence of microwaves.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The search for junctions with high values of the I_cR_n quality factor (with I_c the junction critical current and R_n the normal state resistance) is one of the strong applicative motivations behind the activity on the Josephson effect [1–3]. The I_cR_n product is proportional to the characteristic Josephson frequency of the junction and provides an upper limit for its operation speed, therefore determining clear reference criteria for the applicability of Josephson systems to functional devices. For instance, both superconductor quantum interference device (SQUID) based sensors and rapid single flux quantum (RSFQ) circuits benefit from high I_cR_n products, gaining in maximum magnetic flux resolution and operating speed respectively [4]. RSFQ circuits could be operated at frequencies up to more than 100 GHz, with a power dissipation of only a few per cent of current CMOS transistors. I_cR_n values above the threshold of the meV could extend the functioning of superconducting detectors at the terahertz (THz) frequency making them suitable for many applications such as remote atmosphere monitoring, biomedical research, security and communication technology [5, 6]. THz detectors based on superconductive materials could compete with semiconducting detectors, which are limited in sensitivity and bandwidth. High critical temperature superconductors (HTS), because of their high energy gap values (20 meV in the case of $YBa_2Cu_3O_{7-x}$—YBCO), have given hope of I_cR_n products at least one order of magnitude larger than those obtained using low temperature superconductor (LTS) based junctions. In addition, HTS devices could operate at the liquid nitrogen temperature with nominal I_cR_n products close to the values LTS Josephson junctions exhibit at the liquid helium temperature [7, 8], with a substantial reduction in cost and equipment complexity.

Nevertheless, most of the HTS junctions investigated up to now have given I_cR_n values of the order of a few meV, much lower than expected. This remains as another example of the still debated nature of transport in HTS JJs [9, 10]. The highest values of I_cR_n have been obtained on [100]-tilt bicrystal grain boundary (GB) junctions [11, 12]. In this type of junctions the order parameter might be less suppressed when compared with conventional [001]-tilt junctions, leading to higher J_c values. Bicrystal [100]-tilt junctions have been fabricated both on $SrTiO_3$ (STO) substrates, obtaining I_cR_n values up to 8 mV [11, 13], and low loss $NdGaO_3$ substrates, obtaining I_cR_n values going from 4.5 mV [14] to 8 mV after

an UV oxygenation process [12]. Promising results have also been obtained using step edge junctions and interface engineered Josephson junctions (IEJ) based on low loss MgO and $LaAlO_3$ (LAO) substrates respectively [8]. IEJ devices, in particular, show good uniformity, with low spread of the junction parameters and I_cR_n values up to 5 mV [15, 16].

Off-axis biepitaxial junctions fall in the type of [100]-tilt structures, and as a matter of fact initiated the first comprehensive study on [100]-tilt grain boundaries [17, 18], envisaging possible advantages of this type of structures [9]. In addition, they allow change of the misorientation angles of the junctions on the same chip [18, 19]. This is a relevant property when designing complex electronic devices where junctions with various transport regimes are required. Here we present the properties of high quality off-axis biepitaxial junctions fabricated using low loss substrates, exhibiting I_cR_n values among the highest reported in the literature for HTS junctions [9, 10]. This work responds to the need for a platform of reproducible and high yield HTS junctions also operating at high frequencies.

We have replaced the $SrTiO_3$ (STO) substrates we have been using up to now with commercially available $(La_{0.3}Sr_{0.7})(Al_{0.65}Ta_{0.35})O_3$ (LSAT) crystals. STO is the most commonly used substrate for the realization of YBCO films and devices thanks to the good reticular matching with YBCO, chemical compatibility and structural stability. On the other hand, it has high values of the dielectric constant $\epsilon_r \sim 300$ at 300 K which also increases when lowering temperature up to values in the range of 10^4 [20]. These values are not encouraging for experiments and applications at high frequencies. Moreover, the large stray capacitance of this substrate could introduce a capacitive element in parallel to the junction, making the final circuit structure more complicated [21–23]. The possibility to remove or to better control the stray capacitive element would be important to create a reference system and to better isolate and distinguish transport mechanisms in GBs. Materials such as silicon, sapphire and MgO have good dielectric properties for use at high frequency, but also have poor crystal match with YBCO, requiring for example the use of a buffer layer. Lanthanum aluminate $LaAlO_3$ (LAO) is another material often used for HTS device fabrication. It has lower dielectric constant $\epsilon_r \sim 23$ and lower loss tangent 1×10^{-4} at 77 K, when compared with 6×10^{-2} for STO, while keeping good reticular matching with YBCO. Unfortunately, it undergoes a structural phase transition from rhombohedral to cubic in the temperature range used for the deposition of YBCO thin films [24]. This transition leads to the formation of twin boundaries in the substrate, resulting in stress, roughening of the surface and non-isotropic dielectric properties which will affect the quality of the HTS film deposited on top and, as a consequence, of the junctions [25].

LSAT was developed a few years ago with the aim of combining the low dielectric constant and the low loss tangent of LAO with the structural stability of STO [26]. The values of dielectric constant and loss tangent of LSAT match the ones measured for LAO and are stable in temperature [27]. Moreover, LSAT does not have any known phase transition in the temperature range (4 K to 900 °C) of interest for the realization and use of HTS based devices. An additional advantage is that LSAT substrates are grown using the Czochralski method, which leads to higher quality crystals when compared with the flame fusion method used for the realization of the STO substrates we used up to now [28]. Finally, LSAT has lattice parameter smaller than STO, allowing a decrease of the mismatch with the YBCO film orientations used in the off-axis biepitaxial structure. All these properties make LSAT an excellent candidate for the realization of high quality HTS biepitaxial junctions.

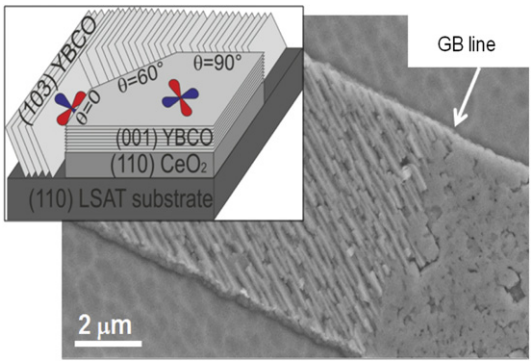

Figure 1. SEM image of a 6 μm wide junction. In the inset a sketch of the junction's structure is shown.

2. Sample fabrication

In off-axis biepitaxial junctions the grain boundary develops where (103) oriented YBCO grains, grown on a (110) oriented substrate, meet (001) grains grown on a (110) oriented seed layer [18, 19, 29]. In this work LSAT has been used as a substrate and CeO_2 as a seed layer. The GB is the result of the following rotations of the crystallographic axes (see inset of figure 1):

- a 45° c-axis tilt, introduced by the rotation of the (001) YBCO cells grown on (110) CeO_2;
- a θ a-axis twist or tilt, depending on the in-plane misorientation between the (001) and the (103) electrode.

The value of the angle θ is defined via the patterning of the seed layer. In the inset of figure 1 the configurations $\theta = 0°$, 60° and 90° are sketched as typical examples. It is possible to realize on the same chip junctions both in the lobe versus lobe configuration (for $\theta = 60°$) which exhibit the maximum critical current, and in the lobe versus node configuration (for $\theta = 0°$, 35 °C and 90°) [19, 29]. The devices shown in this work have been realized by depositing a thin (20 nm) CeO_2 seed layer film via RF magnetron sputtering on a (110) oriented LSAT substrate. The deposition conditions were carefully set in order to obtain fully oriented (110) CeO_2 films. The CeO_2 film was patterned using standard photolithography and Ar ion milling. Then, a 200 nm thick YBCO film was deposited using inverted cylindrical magnetron sputtering leading to a (001) phase on the CeO_2 covered area and a (103) phase on the bare substrate area. This step is crucial: it requires very specific

deposition parameters, which are a compromise between the quite different optimal conditions to separately grow high quality (001) and (103) YBCO thin films. The YBCO film is then covered with a 100 nm gold layer which will protect the superconductor during the following fabrication steps and will also serve for the realization of bonding pads. The junction bridges were defined by standard photolithography and Ar ion milling. During this last step the sample was mounted on a sample holder cooled down to −160 °C using liquid nitrogen in order to minimize the loss of oxygen. Another step of photolithography and cold ion milling was finally required for the realization of bonding pads and the removal of the protective gold layer. A structural and morphological characterization of the thin films deposited, both CeO_2 and YBCO, has been carried out using several techniques. X-rays diffractometry shows that samples grown on LSAT have high epitaxy and no significant differences in the crystalline quality could be found comparing with the samples grown on STO. From the morphological point of view, on the other hand, atomic force microscopy (AFM) and scanning tunnel microscopy (SEM) analyses have shown that the quality of the YBCO films obtained using LSAT as a substrate is extremely high. A scanning electron microscope (SEM) image of a typical junction is shown in figure 1. By the comparison with the results obtained in the past on STO substrates (see for example the SEM images shown in [18, 29]) it is clear that the (001) YBCO phase is more uniform, with a lower density of impurities and holes, and the (103) phase has larger, better defined grains. This morphological analysis is a first, indirect indication of a better uniformity of the GB, which is confirmed by the transport measurements we will show in section 3.

The devices presented in this work have a width of 6 μm and misorientation angles θ from 0° to 90°. They were measured in a shielded environment using a standard four terminal configuration down to 0.3 K. The measurement system was also equipped with resistor–capacitor (RC) filters with a cut-off frequency of 1.6 MHz and lowpass copper-powder filters with a cut-off frequency of 10 GHz for the reduction of electrical noise.

3. Transport properties

In figure 2 some typical current versus voltage (IV) characteristics are shown. They encompass the two extreme and most significant cases of hysteretic and not hysteretic behaviors, signifying relevant tuning of the capacitive effects. The presence of hysteresis in biepitaxial junctions on a low dielectric substrate confirms that the GB microstructure and the nature of the junctions are the main causes of the capacitive effects.

The capacitance C can be calculated from the junction's hysteresis using the expression for the Stewart–McCumber parameter [2]: $\beta_c = 2\pi I_c R_n^2 C/\Phi_0$, where Φ_0 is the magnetic flux quantum, and equating it to the β_c obtained by the Zappe approximation [30]: $\beta_c = [2 - (\pi - 2)\alpha]/\alpha^2$, where α is the ratio between the return current and the critical current. Another way to calculate the capacity is to use the voltage position of the Fiske steps [2]. These are due to the resonance

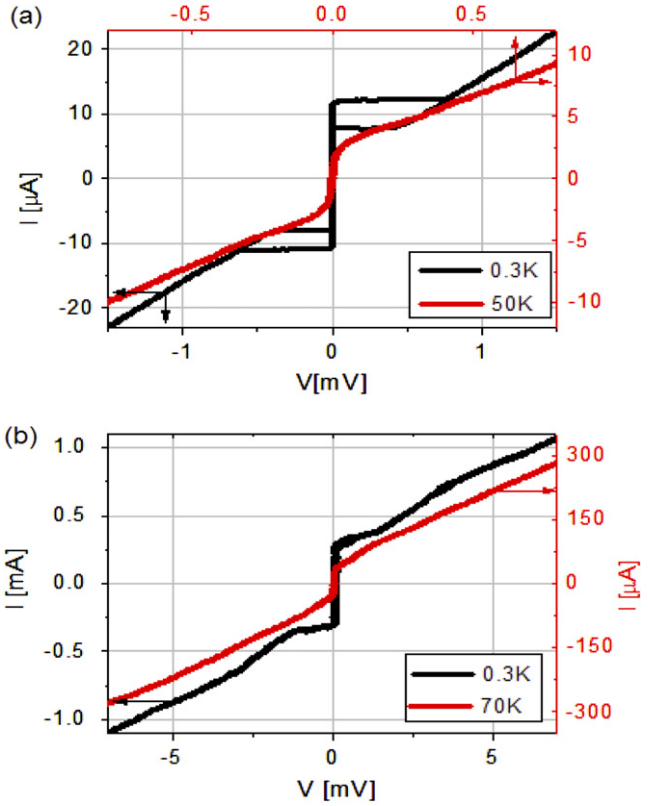

Figure 2. Typical IV characteristics at different temperatures in the case of large (a) and negligible (b) hysteresis.

of an electromagnetic wave propagating in the barrier. The voltage position of the nth order resonance V_n is given by $V_n = \frac{n\Phi_0\bar{c}}{2w}$, where w is the junction width and $\bar{c}$ is the phase velocity of the electromagnetic wave. $\bar{c}$ is connected to the junction's barrier thickness t:

$$\bar{c} = c_0\sqrt{t/\epsilon d}, \tag{1}$$

where c_0 is the velocity of light in vacuum, ϵ is the relative dielectric constant and $d = t + \lambda_L + \lambda_R$ is the magnetic width of the barrier, with λ_L (λ_R) being the London penetration depth of the left (right) electrode. In our case, $\lambda_L + \lambda_R = \lambda_{001} + \lambda_{103} \simeq \lambda_{103} = 2$ μm [31]. The capacitance per unit area can be therefore calculated as $c = \epsilon_0\epsilon/t$. For the devices studied in this work, the two methods of estimation lead to capacitance values which differ by up to two orders of magnitude, similarly to what has been found for other types of GB junctions (see for example [32] on bicrystal junctions). The difference in the capacitance values found in the experimental data suggests a picture of a barrier where different levels of oxygenation and disorder, along the transport channel and in the proximity of the GB region, may possibly contribute to the overall capacitance in different ways (see figures 4(b) and (c)). Fiske steps and hysteresis are indeed probably sensitive to different active regions, the former being induced by wave propagation along the crystallographic GB area and the latter taking into account also nearby areas [32, 33].

In figure 3 the specific capacitance values c as a function of the critical current density of the junctions described in

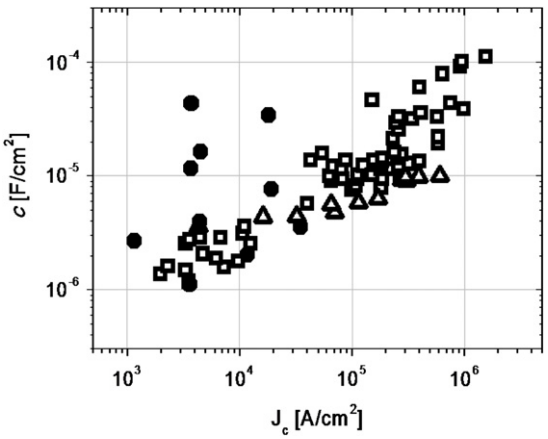

Figure 3. Specific capacitance versus J_c of the off-axis biepitaxial junctions described in this work (filled dots) compared with data of various types of GB junctions reported in [33, 10] (open squares) and with data of IEJs reported in [16] (open triangles). All the capacitance values were calculated from the Fiske resonance positions.

this work (filled dots) are compared with data from [10, 13] (open squares) referring to GB junctions produced by a variety of techniques on various types of substrates (including STO, MgO and LAO) and with data from [16] (open triangles) referring to interface engineered junctions realized on LSAT. The data of this work refer to junctions with different interface orientations, which leads to microscopic change in the barrier (see also the following paragraph) and to some spread of the J_c values [19, 29]. From these data it is possible to see that off-axis junctions exhibit specific capacitance values which are on the average higher than other types of junctions. Values of specific capacitance of off-axis biepitaxial junctions on STO substrates are about 5×10^{-4} F cm^{-2} [29], one order of magnitude larger than those found in this work for LSAT based junctions. We have calculated the values of t/ϵ using equation (1): for the junctions on LSAT the average value is $t/\epsilon = 0.3$ nm whereas for STO based junctions it is two orders of magnitude smaller. These values are in substantial agreement with what has been reported in the literature [22] and indicate that in the case of LSAT junctions, the effect of the substrate stray capacitance is negligible. We point out that also in the case of traditional [001] bicrystal junctions, a difference of a factor of ten is found when comparing the values of the specific capacitance of STO substrate based devices with MgO and LAO based ones [22]. In conclusion, LSAT off-axis biepitaxial junctions, although having a specific capacitance lower than the same junctions based on STO, still have specific capacitance higher than other types of junctions (in particular in-plane junctions).

In figure 4(a) representative values of the I_cR_n product extracted from IV characteristics are shown as a function of the J_c, all measured at 0.3 K (black dots). The I_cR_n values are on the average extremely high, with a maximum value of 12 mV. These are among the highest I_cR_n values reported in the literature for GB junctions and the main result of this work. In figure 4 data from other types of YBCO Josephson junctions are also shown. When comparing data with similar J_c, LSAT based junctions show I_cR_n values which are about one order of magnitude higher. High I_cR_n values are also measured at high temperature, with values of 1 mV at $T = 70$ K (see figure 2), which is extremely encouraging for applications. These junctions seem to benefit from an increase of J_c when compared with off-axis biepitaxial junctions on STO substrates, while R_nA values ranging from 10^{-6} to 10^{-7} Ω cm^2 are close to those measured in all other junctions of the same type. These are typically larger than values measured in 'in-plane', [001]-tilt GB junctions.

In GB junctions, the I_cR_n product and the J_c are found to be linked by the relation $I_cR_n \propto J_c^q$ [9, 10, 35, 34, 36], although there is no general consensus on the exact value of q, which experimentally ranges between 0.4 and 0.7, nor on the real meaning of this scaling law. Looking at the graph of figure 3, a marked difference with most data available in the

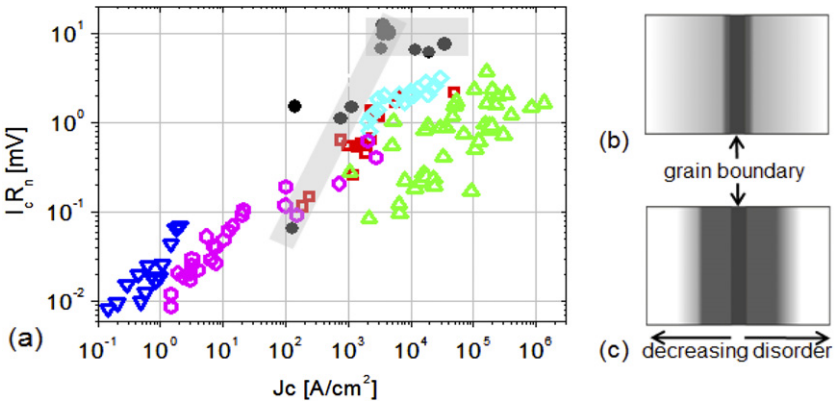

Figure 4. (a) Scaling behavior of I_cR_n versus J_c for the biepitaxial junctions described in this work (black dots), compared with data of off-axis biepitaxial junctions fabricated on STO (open red squares) [29], bicrystal junctions (open green triangles) [35], ramp edge junctions (open blue down triangles), step edge junctions (open cyan diamonds) and (103) trilayers (open magenta hexagons) [9, 36]. The data on biepitaxials (black dots) refer to junctions with various misorientation angles. We show also sketches of a uniform barrier composed of only one region, highly disordered corresponding to the crystallographic GB (panel (b)), and of a barrier where the GB is surrounded by two adjacent areas with decreasing disorder, penetrating into the adjacent electrodes (panel (c)). In the case (c) all the areas contribute in series to the transport.

literature is evident: a saturation of $I_c R_n$ at 10 meV is found for J_c values above $J^* = 5 \times 10^3$ A cm^{-2}.

A similar plateau, but for lower values of the $I_c R_n$ product, has been reported in the past studying the effect of GB oxygenation via ozone annealing and electromigration in GB bicrystal and interface engineered junctions. In [37], $I_c R_n$ was found not to depend on J_c after annealing treatment in ozone, and explained in terms of a junction's barrier composed of various regions. The region of the crystallographic GB is the less transmissive and more disordered part and is surrounded by areas where such disorder gradually decreases (figure 4(c)). The ozone oxygenation process restores the oxygen content in the less disordered areas extending in the electrodes, while the crystallographic GB remains unaltered. Therefore, after annealing the barrier is reduced to the crystallographic GB only (figure 4(b)) and the transport properties will be dominated by this area. The plateau in the $I_c R_n$ versus J_c behavior is a fingerprint of a more uniform barrier 'localized' at the GB. This happens for J_c values greater than $J^* = 5 \times 10^3$ A cm^{-2}. For J_c values lower than J^*, other regions are probably added in series to the central GB area, and are responsible for the scaling behavior of the $I_c R_n$ versus J_c and for the different values of the capacitance calculated from the hysteresis and from the Fiske steps position. LSAT substrates seem to favor a more uniform barrier region where the influence of possible charge trapping is significantly reduced.

The analysis of the transport properties described in this work fits well the band bending model [9, 10, 38]. In this scenario, the structure of the GB barrier in HTS junctions is approximated by three adjacent layers: one in the middle, where most of the structural disorder is concentrated, and two neighboring layers where the electronic properties of the superconductor are electronically affected by the GB interface. Both Cooper pairs and quasi particles would tunnel through such a barrier, directly or with a multi step process. In [38] several junction parameters' are estimated using this model. Specific resistance $R_n A$ is found in the range of 2×10^{-6} Ω cm^2 and the specific capacitance c in the range 1.2×10^{-5} F cm^{-2}. These values are consistent with the experimental data of the present work. The band bending model has been considered for the explanation of the noise properties of another case of [100]-tilt junctions (having a bicrystal structure) realized on low loss substrate and exhibiting high $I_c R_n$ values [12].

The central theme of the paper, i.e. the possibility to reduce charge trapping at the GB with a consequent increase of $I_c R_n$, holds regardless of the details of the GB microstructure. Intrinsic effects, such as the specific microstructure of the GB when changing the interface orientation or the influence of the order parameter [19, 29], and extrinsic effects such as faceting [10, 39, 40] determine some scattering of the data in figures 3 and 4 without affecting the general trends. We expect more quantitative insights into these additional effects from the study, currently in progress, of submicron junctions.

4. Conclusions

High quality off-axis biepitaxial junctions on LSAT substrates have been fabricated. The fabrication process of the samples presented here, including the choice of LSAT as substrate material, was tuned in order to obtain high quality junctions with a uniform microstructure. A significant increase of the $I_c R_n$ product, up to 12 mV at 0.3 K and 1 mV at 70 K, comes out as a consequence of an improved barrier uniformity.

The high values of the $I_c R_n$ product, in conjunction with the use of a low loss substrate, are of great interest for electronic applications, such as for example the realization of RSFQ circuits and devices and sensors to be used at high frequency.

Acknowledgments

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