Single flux quantum comparators for HTS AD converters

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Abstract

We have investigated different comparators for Flash and $\Sigma-\Delta$ high temperature superconducting ADCs designed using three-layer HTS tri-crystal junction integrated circuit technology with spread of the junction critical currents less than 10% and features size 0.6 μm. Using the theoretical estimations for the bit error rate in RSFQ circuit under the restrictions of the given technology, we have estimated working temperature as $T = 62$ K. At this temperature, the circuits were optimized in order to achieve maximum performance of the related ADCs in terms of input bandwidth, resolution and operating margins. For design purposes, a novel method was developed for inductance calculation with 3D magnetic field distribution in multilayer superconducting technology and extraction of the inductance matrix of the equivalent circuit. © 1999 Elsevier Science B.V. All rights reserved.

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1. Introduction

There is a vast number of conceivable circuit designs for A/D converters. The most popular of them are: integration types, counter types and parallel types. Each approach has characteristics that make it most useful for a specific class of applications, based on speed, accuracy and hardware cost.

From the general structure of the A/D converters we can extract two components that mostly define the key properties of conversion — analog signal conditioner and comparator. Analog signal conditioners (''analog-to-analog'' converters) are used to make the input signal suitable for conversion. Analog comparators make an elementary choice between the magnitude of two inputs and decide which is greater. This is the equivalent of a one-bit A/D conversion. The A/D conversion process usually calls for a number of decisions; they may be made sequentially by a single comparator or simultaneously by a whole string of comparators, as in ''flash'' converters.

The accuracy (in fraction of LSB), a number of effective binary bits N, linearity, and speed (input

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bandwidth f) are primarily affected by the properties of the comparator and signal conditioner. The dependence between N and f for the sine-wave reference signal is given by the following equation, where T is the conversion time:

$$f = \frac{1}{T2^{-N}}. \tag{1}$$

In superconductive circuitry, the analog signal conditioners are naturally realized using the effect of magnetic flux quantization. This effect means that in a superconductive loop broken by Josephson junctions there is a circulating current which is a function of the applied magnetic flux. There are many different signal conditioning circuits employing magnetic flux quantization depending of the ADC type and type of the digital code. It can be, for example, Quasi One Junction SQUID (QOJS) [1] or double junction interferometer [2] or $\Sigma{-}\Delta$ modulator [3].

In any case, the circulating current has to be sampled to determine its direction. One direction is arbitrarily assigned as digital ''0'' and the other as digital ''1''. In the most modern designs, a serial connected pair of overdamped Josephson junctions (balanced comparator) [4] electrically coupled with the input loop is used for digitizing purposes. The output digital signal is in the form of single flux quantum (SFQ) pulses [5] that can be further processed with RSFQ superconductive digital devices [6].

In the last 10 years, the great progress was achieved in understanding and designing superconductor A/D converters. The best-reported performances of superconducting low temperature ADCs currently are 14 bit, 20 MS/s for counter type [7] and 6 bit, 10 GS/s for flash type [8].

The speed of SFQ circuits is determined by the $I_c R_n$ product of the employed Josephson junctions. For currently standard 2 μm niobium process the characteristic time constant is typically ≈ 6 ps and decreases linearly with minimum linewidth. During the last 5 years, significant effort was made to establish niobium technology with submicron Josephson junctions. Up to now only single cells with few junctions were experimentally tested and the best achievement is a T Flip-Flop operating up to

750 GHz with 2 mA/μm^2 critical current density of the Josephson junctions [9].

Another very prospective approach is to use high-temperature superconductor (HTS) Josephson junctions. These junctions exist in various types but in general they have very high $I_c R_n$ up to 8 mV [10] at the helium temperature and natural non-hysteretic $I{-}V$ curves. This means that characteristic time constant T can be rather small close to ≈ 200 fs. But to realize A/D converter in high-T_c technology is not an easy feat due to a number of theoretical and technological restrictions that are related to the nature of the high-T_c Josephson junctions. Up to now there have been done only a number of demonstrations of HTS digital circuits in a level of the 10–20 junctions [11,12]. Most of them were created in bicrystal technology providing reasonable spread of the critical currents.

In this work, we investigate different comparators for flash and $\Sigma{-}\Delta$ high temperature superconducting ADCs designed using three layers HTS tri-crystal junction integrated circuit technology. This work was done through the following steps: optimization of the circuits without noise and technology restrictions on inductances, theoretical calculation of the bit error rate (BER) and comparators current sensitivity in a presence of thermal noise, reoptimization with the inductances extracted from the layout. In conclusion, general restrictions on the HTS technology for RSFQ circuits are discussed.

2. Comparators optimization

A typical circuit of SFQ-driven converter with balanced comparator is composed of three parts (see Fig. 1): clock pulse input driver, balanced comparator and output pulse conditioner. SFQ clock-driven pulses with frequency f_{samp} are passed through the JTL to the interferometer {$J7$, $J6$, $J3$, $J2$} that includes the balanced comparator formed by junctions $J3$, $J2$. Each pulse induces a 2π-leap of the Josephson phase in either junction J_2 or junction $J3$, depending on whether the measured current I_{sign} is larger or smaller than a threshold I_t. The switching of the $J2$ junction means that a SFQ pulse is
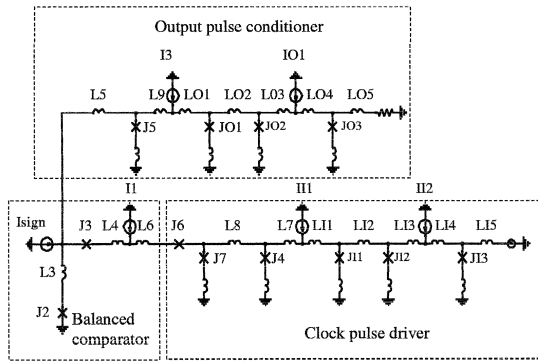
Fig. 1. Equivalent circuit of the typical SFQ-driven converter with balanced comparator.

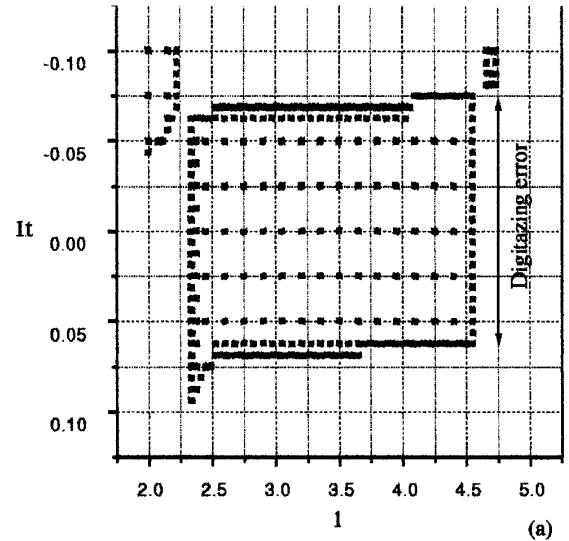developed across it. This pulse then passes the output conditioner that amplifies its energy.

There is also a region in parameter space where both junctions of the comparator can switch simultaneously. This effect leads to some uncertainty of the threshold ΔI_t and also to the appearance of extra flux inside the input interferometer that will affect the sample pulse propagation. Typically the effect of double switching can be avoided during optimization, but it still occurs (as it will be shown later) in the HTS case where the parameters are limited by hard technology restrictions. In order to avoid propagation of the SFQ pulse back to input JTL in case of double switching of junctions $\{J2, J3\}$ junction $J6$ is added into the circuit.

The circuit has been simulated and optimized to find working parameters correspondent to peak performance conditions: maximum operational frequency, minimum threshold uncertainty and the largest parameter margins. All simulations were done with the help of the PSCAN program [13] in values normalized on the critical current of the smallest Josephson junction $I_c^{\min}$ and $I_c R_n$ product. The values of inductances and resistors are normalized correspondingly on the $\beta_1 = \Phi_0 / 2\pi I_c^{\min}$ and $I_c R_n / I_c^{\min}$.

The optimization was done under the condition that the measured signal is a linear function of the time within the range $\pm I_c^{\min}$. It was found that maximum operational frequency is about $f_{\text{samp}} = 0.06$ ω_c and limited rather by the switching time of the input interferometer then the errors in comparators

switching. At this frequency, the threshold uncertainty or digitizing error in terms of AD conversion can be found varying the current increasing rate. As is shown in Fig. 2, the final threshold uncertainty is less than 5% of $I_c^{\min}$. All circuit parameters (Fig. 2(b)), except critical currents of the decision making pair, have margins larger than 30%. The margins for critical currents of the Josephson junctions in the balanced comparator are not higher than 3%. This means that a small distortion of the balance between these two junctions strongly influences the threshold and its uncertainty.

In order to investigate the performance of the QOJS comparator, we have used the same circuit connecting the balanced comparator with QOJS loop $\{J1, L1\}$ (see Fig. 3). Therefore, the signal current to

(a)

I1=3.36	II1=4.76	I3=1.57
I2=3.15	IO1=2.45	Ioff=0.18
J2=3.80	J3=3.80	J4=3.80
J5=1.00	J11=2.99	JI2=2.50
J13=2.00	J7=3.80	J6=2.88
JO1=1.25	JO3=2.00	JO2=1.50
L3=0.01	L4=0.60	L5=3.52
L7=0.37	L9=1.50	LI1=0.50
LI2=1.20	LI3=0.60	LI8=0.09
LI4=0.75	LI5=1.50	LO2=2.25
LO1=1.20	L8=0.75	LO4=0.75
LO3=1.12	L6=0.09	Lp=0.01

(b)

Fig. 2. Digitizing error of balanced comparator at clock frequency $f = 0.06$ ω_c (a) and table of optimum working parameters (b).
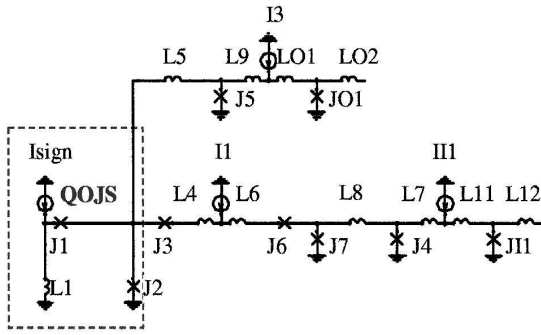
Fig. 3. Equivalent circuit of the QOJS comparator with SFQ sampling.

be sampled by the balanced comparator is the current through junction $J1$ in the QOJS interferometer. For the linear reference input signal the current I_{J1} is a periodic function of analog input current with the period $\Phi_0/L1$ and mean value equal to zero. The parallel combination of the N QOJS comparators can be naturally applied for construction of the flash type ADC with N effective bits gray coding of the digital data [14].

There is a dynamic hysteresis in the current phase characteristic of QOJS. It was shown in Ref. [15] that the width of hysteresis became smaller for larger ration I_{c2}/I_{c1} and smaller parameter $\beta_1 = \Phi_0/2\pi I_{c1}L1$. This width should be kept smaller than half of the period of the loop current in order to have the accuracy of the ADC less than $1/2$ LSB. Under this condition we have found the dependence between frequency of the input current and β_L for linear reference signal with amplitude $\Phi_0/L2$ and ratio $I_{c2}/I_{c1} = 3$ (see Fig. 4(a)). As a result, for LSB comparator the maximum input frequency that corresponds to $\beta_L = 0.4$ is close to $\approx 0.014 \ \omega_c$ (Fig. 4(b)).

With the obtained maximum input frequency and QOJS parameters ($I_{c2}/I_{c1} = 3$, $\beta_L = 0.4$) the remaining part of the circuit operates with the parameters calculated for the balanced comparator itself.

For obtained maximum input signal frequency for LSB comparator, the relation between resolution of ADC and input bandwidth is given by Eq. (1). For typical value of $I_c R_n \approx 2$ mV for HTS Josephson junctions, the maximum LSB frequency is ≈ 176 GHz that will give maximum bandwidth of flash

type ADC not higher than $f = 2$ GHz with resolution of $N = 6$ bits.

The same procedure was followed for investigation of a $\Sigma-\Delta$ modulator (see Fig. 5(a)). Following the approach of Przybysz [3], a $\Sigma-\Delta$ modulator was constructed as a combination of superconductive inductor $L1$ and resistor $R1$. The current to be sampled by the balanced comparator is the current through the inductor I_{L1}. In the ideal case with high accurate sampling for constant input signal I_{sign} the current I_{L1} is a periodic function of time with period $T = \Phi_0/I_{sign}R1$ and amplitude $\Phi_0/L1$ (Fig. 5(b)).

We have simulated $\Sigma-\Delta$ with $R1 = 0.005$, $L1 = 2$ and input frequency equal to $f = 2.1 \times 10^{-3} \ \omega_c$. The circuit has demonstrated correct operation with the parameters obtained for the balanced comparator.
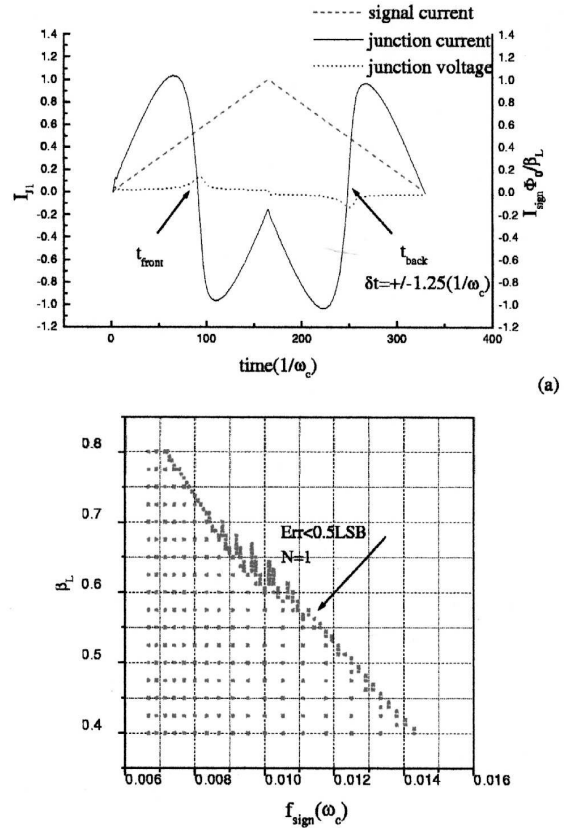

(a)

Fig. 4. Definition of the hysteresis width of $I_{J1}(t)$ dependence in QOJS (a) and maximum input frequency f_{sign} for 1-bit flash ADC with the accuracy less than $1/2$LSB as a function of QOJS β_L (b).
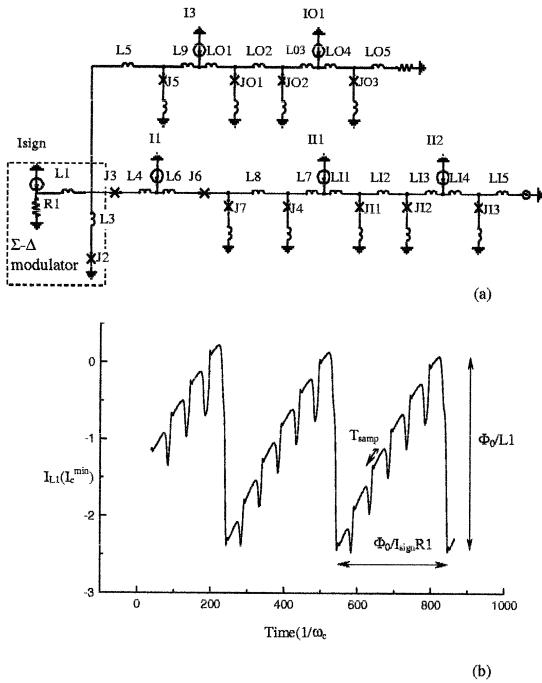
(a)

(b)

Fig. 5. Equivalent circuit of the $\Sigma - \Delta$ modulator with SFQ sampling (a) and time dependence of the current in the quantizing loop for constant input signal (b).

The resulting oversampling ratio for the maximum input frequency and maximum sampling frequency is $f / f_{samp} = 24$.

3. Technology process

The fabrication sequence used consists of (1) substrate alignment markers etching for determination of the grain boundaries positions, (2) YBCO film and in-situ gold film deposition, (3) gold deposition for e-beam lithography markers, (4) YBCO e-beam patterning, (5) dielectric deposition and e-beam patterning, and (6) gold deposition and e-beam patterning for bias resistors and contact pads. The substrate material is a YSZ. Each substrate contains three symmetric bicrystal lines with missorientation angle $\alpha = 24°$. The alignment markers were patterned in the substrate using ordinary photolitography and ion-beam milling techniques. The positions of these markers to the grain boundary lines were obtained with an accuracy of about 1 μm. YBCO

thin films with 200 nm thickness were deposited using a laser ablation technique at oxygen pressure (0.3 mbar) and temperature (730°C). An in-situ Au film of 20 nm thickness was deposited using the laser ablation method to provide protection from air of the YBCO film, followed by a thick 200 nm Au film obtained by the e-beam evaporation system. Patterning of the microbridges through the grain boundary lines (Josephson junctions) and the circuits geometry was made using e-beam lithography and ion-beam milling with feature size 0.6 μm. Resistive lines and contact pads were fabricated from Au and insulated from the YBCO pattern by an amorphous CeO_2 insulating layer, obtained by laser ablation technique.
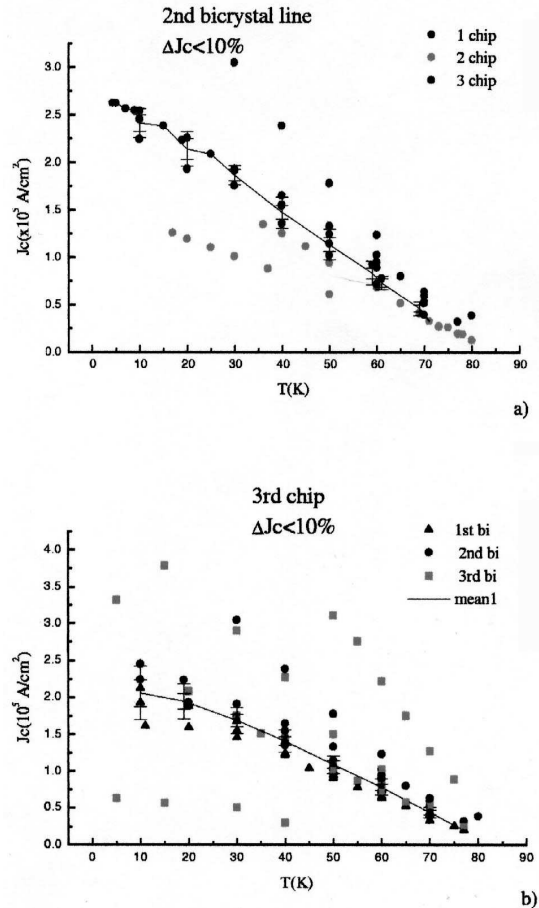

a)

b)

Fig. 6. Comparison of the $J_c(T)$ dependencies of the 24° bicrystals junctions between three test chips (a) and between three grain boundaries on the one chip (b).

Under equal conditions, three chips were fabricated with the test structures containing 24 Josephson junctions per chip (eight junctions per each grain boundary) with linear size $w = 2$–8 μm. We have tested 36 junctions from all the chips and found that with yield of 13% perfect RSJ like behavior can be observed under the conditions $w < 4\lambda_J$. The resulting spread of the J_c and R_n between different grain boundaries and between different chips is not higher than 10%. The average critical current density at helium temperature is equal to J_c (4.2 K) $= 2.5 \times 10^5$ A/cm^2 and is a linear function of temperature (see Fig. 6). The average value of the $I_c R_n$ product is equal to 3 mV (4.2 K).

4. Thermal noise analysis

It is important that all key parameters of the circuit such as working temperature, minimum critical current I_c^{min}, $I_c R_n$ and minimum inductance of the loop are defined only by the BER. For most general purpose applications, the level of the BER can be taken as 10^{-16} 1/bit. This means that circuits with integration of about 10^3 bits with operational frequency of about 20 GHz will work without any fault during at least 8 min.

A theoretical analysis was developed [16] that is based on the consideration that in general the influence of noise in RSFQ circuits can be estimated from the probability P of error switching in a pair of junctions in a balanced comparator:

$$P = 1 - \mathrm{erf}\left(\sqrt{\pi}\,\frac{I_t - I}{\Delta I_t}\right), \tag{2}$$

where ΔI_t is the effective threshold uncertainty and $(I_t - I)/I_c$ can be considered as a margin for critical current. The effective threshold uncertainty ΔI_t depends of many parameters and in particular of clock driver output impedance $Z(\omega)$. For HTS circuits based on bicrystal junctions because of large inductances one can apply results of theory in the thermal fluctuation and low speed operation $(|Z(\omega)| \gg R_n)$ limits.

$$\Delta I_t\,[\mu A] = 23 \times 10^3 \left(\frac{2\pi k_B T}{\Phi_0}\right)^{2/3} I_c^{1/3}\,[\mu A]. \tag{3}$$

Therefore, the relationship expressed in Eq. (2) and Eq. (3) gives the value of the BER as a function of $k = I_c/T$ (in units [μA/K]).

Under the restriction of the given technology there are three fixed parameters that will define the k parameter: critical current density J_c (4.2 K) $= 2.5 \times 10^5$ A/cm^2, film thickness $d = 0.2$ μm and liner size of the Josephson junctions $w > 2$ μm. From the $\lambda_J(T)$ dependence, restriction that $w < 4\lambda_J$ and critical currents need to be varied between 1 and $2I_c^{min}$ follows that minimum working temperature should be higher than $T = 62$ K. At this temperature, the critical current of the smallest Josephson junction is equal to $I_c = 300$ μA that corresponds to the $k = 4.83$ [μA/K] and through Eq. (2) (with margins 30%) to BER $\approx 10^{-14}$.

As a result, the estimated working temperature is $T = 62$ K and corresponding units of current and voltage in the simulation are respectively 300 μA and 420 μV, resulting in units of resistance, inductance, frequency and time which are respectively 1.4 Ω, 1.09 pH, 1.27 THz, 0.78 ps.

5. Comparators design

Several circuits were suggested for low-frequency and high-frequency ''dc'' experimental investigations of comparators based on bicrystal Josephson junctions: balanced comparator, QOJS comparator with SFQ sampling, QOJS comparator with dc sampling, Σ–Δ comparator.

Following the same line as was done for the simulations of the different comparators, all circuits have the similar element, balanced comparator. For low frequency experiment, there are also included
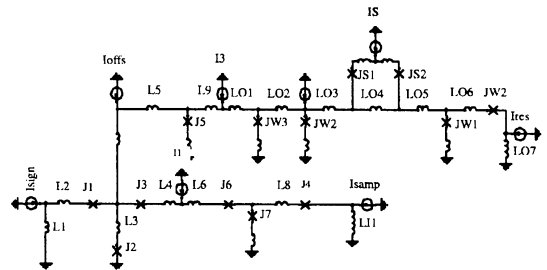

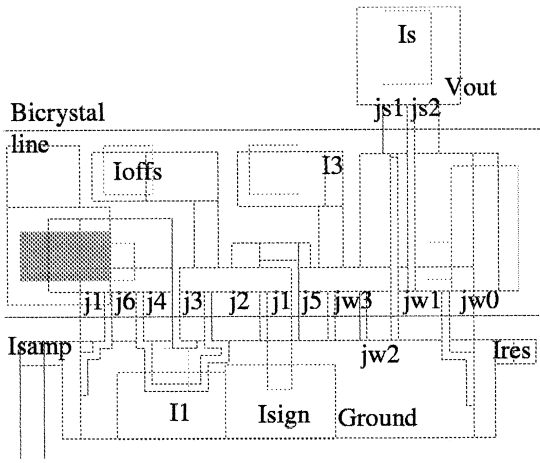Fig. 7. Equivalent circuit for QOJS comparator low frequency testing.

Fig. 8. Layout of the QOJS comparator with SFQ sampling based on HTS bicrystal Josephson junctions.

dc/SFQ and SFQ/dc converters. Following the approach in Ref. [11] we have realized the SFQ/dc converter as a double junction SQUID-driven by the SFQ pulses. This approach requires an additional external control signal for reset operation of the SQUID. The number of junctions was reduced to the smallest possible value in order to maximize circuit yield.

The typical equivalent scheme of the experimental circuits (QOJS with SFQ sampling) for low-frequency testing is presented in Fig. 7. Under the design rules developed for given technology, the layout of the circuits was created. In Fig. 8, the corresponding layout is shown. In these circuits, Josephson junctions are formed as the microbridges with the minimum length 3 μm over the bicrystal lines. Therefore, a double junction interferometer is formed as a plane loop around the submicron slit in the superconductive film.

In these structures, magnetic field is essentially 3D in nature. The kinetic inductance can be compared with magnetic energy inductance because the

values of the London penetration depth are compared with the thickness of the layers and rapidly increase with working temperature. These facts significantly hamper accurate inductance calculations for such devices and practically exclude the application of existing software. In order to overcome the difficulties, a new program 3D-MLSI (3D MultiLayer Superconducting Inductances) for inductance extraction was developed (see Appendix A).

With the help of this software package, the inductances in the equivalent circuits were extracted (see Table 1). Due to the absence of a ground plane and a number of topology restrictions, the calculated minimum loop β_1 was about ≈ 5. The simulation with the extracted large inductances demonstrated that a large value of the β_1 parameter leads to the possibility to store one or more flux quanta inside the balanced comparator loop. This affects the performance of the comparators. As a result, the maximum sampling frequency was decreased to $f_{samp} = 0.01$ ω_c with the same accuracy of digitizing and operational margins of only 15%.

6. Conclusion

We have investigated the properties of the QOJS comparator and Σ–Δ modulator for the RSFQ A/D converters. Optimization without influence of noise and restrictions on the inductances, the circuits demonstrated correct operation up to sampling frequency $f_{samp} = 0.06$ ω_c with 30% margins of the circuit parameters. The digitizing error for both circuits is about 5% of minimum critical current. The maximum input frequency of the LSB of flash type A/D converter was determined as a function of β_L of the QOJS comparator loop that corresponds to the $f_{sign} = 0.014$ ω_c ($\beta_L = 0.4$).

A HTS integrated circuit technology with Josephson junctions that are formed across three parallel

Table 1
Extracted from layout parameters of QOJS with SFQ sampling

L4 = 2.02	L6 = 3.46	L1 = 3.9	L2 = 4.77	L5 = 2.41	L7 = 0.0
L9 = 0.875	L10 = 1.183	LS1 = 2.85	LS2 = 2.91	LW0 = 3.8	LW5 = 0.875
LW4 = 1.57	LW3 = 2.24	LW2 = 2.24	LW1 = 2.56	LW10 = 3.12	J1 = 1
J2 = 2	J3 = 1	J4 = 1.2	J5 = 1.2	J6 = 1.0	JW0 = 1
JW3 = 1	JW1 = 1.8	JW2 = 1	I1 = 0.8	I3 = 1.09	IS1 = 1.69

24° grain boundaries placed 20 μm apart on (Y)ZrO$_2$ substrates was developed. The quality of the Josephson junctions was tested on three chips with 32 junctions on each and a spread of less than 10% in junction critical current was determined.

The analysis of the circuit noise immunity based on the given technology parameters (J_c (4.2 K) = 2.2×10^5 A/cm^2, $I_c R_n$ (4.2 K) = 3 mV) showed that operational temperature for the designed circuit can be up to 62 K with BER 10^{-14}.

Under the established design rules, several circuits were designed for low-frequency experimental investigation of the comparators. The inductances of the equivalent circuits were extracted with the help of a newly developed method of inductance calculation in 3D-distribution of magnetic field. Due to the absence of a ground plane and a number of topology restrictions, the calculated minimum loop β_1 was about ≈ 5.

The simulation with the extracted large inductances demonstrated changing of the circuits dynamics that affected the performance of the comparators. As a result, the maximum sampling frequency was decreased to $f_{\mathrm{samp}} = 0.01 \ \omega_c$ with the same accuracy of digitizing and operational margins of only 15%.

As a result, we can once more confirm the already known statement that HTS bicrystal technology is not suitable for fabrication of highly integrated RSFQ devices operated at high frequency. However, this technology allows one to investigate some basic properties of rather simple circuits and to check the correctness of design tools and approaches that are developed.

There are a few alternative HTS technologies [3,10] suitable for fabrication of RSFQ circuits with small inductances and higher operational frequency. High frequency operation, however, demands much higher critical currents to compensate the thermal noise.

In case of high speed operation with small value of input impedance $Z(\omega) \ll R_n$ the threshold uncertainty in the balanced comparator is given by the following equation [16]:

$$\Delta I_t [\mu\mathrm{A}] = 10^3 \left(2\pi \frac{2\pi k_B T}{\Phi_0}\right)^{1/2} I_c^{1/2} [\mu\mathrm{A}]. \qquad (4)$$

In that case, the coefficient $k = I_c / T$ μA/K is considerably larger and leads to a high value of the

junctions critical currents. For example with BER = 10^{-16} ($k = 32$) and temperature $T = 40$ K, the critical current should be $I_c = 1.2$ mA.

One can calculate the maximum critical current that can be reached in a given technology assuming that linear dimensions of the junctions are equal to $4\lambda_J$. This critical current is independent of critical current density and given by following equation:

$$I_c^{\max} = 16 \lambda_J^2 J_c = 16 \frac{\Phi_0}{2\pi d_I \mu_0}, \qquad (5)$$

where d_I is a magnetic space between two electrodes and in most cases can be taken as $2\lambda_L$. From Eqs. (2) and (5) follows the relation between maximum working temperature and k (or correspondent BER). This dependence for typical HTS parameters ($T_c = 86$ K, $\lambda_L = 0.2$ μm) is presented in Fig. 9 under the condition that in the circuit Josephson junctions have a normalized critical current between $1 I_c^{\min}$ and $3 I_c^{\min}$.

Therefore, we have found that the desired value of BER defines the operational temperature that in turn defines the minimum critical current being used during optimizations. Area of the largest junction is defined by $4\lambda_J$ and is a function of critical current density J_c. If it is possible or not to reach the obtained working temperature depends on the technology capabilities in junction sizes and J_c. For example, for BER = 10^{-16} and corresponding $k = 32$ μA/K the maximum working temperature is $T = 27$ K, and the minimum value of the critical current is
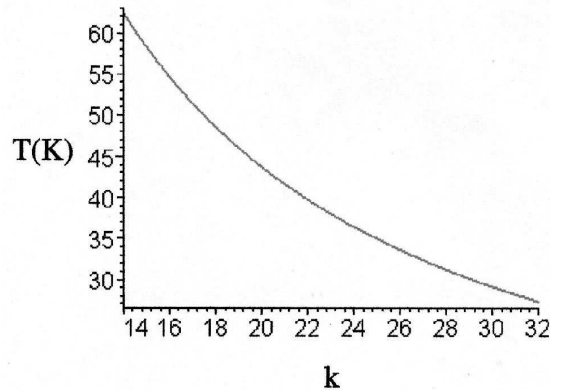

Fig. 9. Working temperature for RSFQ HTS circuits as a function of $k = I_c / T$ defined by BER.

$I_c^{\min} = 864$ μA. For standard photolitography feature size of 2 μm the latter corresponds to $J_c = 20 \times 10^3$ A/cm^2.

Acknowledgements

Appendix A. Equivalent circuit inductances extraction

The program package 3D-MLSI is based on a new mathematical model. This mathematical model is derived from the London equations and takes into account planarity of the structure, finite thickness of layers of metallization and dielectric, and 3D structure of magnetic field. The superconductivity current density is presented by use of a potential representation called stream function or T-function. The stream function is a single scalar unknown function in the problem. The full and correct setting of the boundary value problem for integro-differential equations for stream function is obtained. The terminal currents and currents circulating around holes in superconductors are introduced by simple boundary conditions of the first kind in a way similar to boundary conditions for the Laplace equation. The matrix of self- and mutual-inductances is introduced by use of the functional of full energy. The same inductance matrix allows one to calculate fluxoids.

For the numerical solution of the problem, the finite element method on a triangular mesh with linear finite elements is used. For these finite elements, the current density is simulated by circulating currents with piecewise-constant density. The program package contains a powerful triangular mesh generator. More information about mathematical model, numerical technique and examples of calculations can be found in Refs. [17,18].

An important part of the program package is the preprocessor part. The structure of input data is very rich and flexible and allows us to calculate large and complicated devices. In order to solve the problem to import the shape of conductors and other parameters from layout data presented in certain CAD form, we have developed a converter from DXC format [19] data to internal 3D-MLSI format. The converter can parse the physical layers sequence and extract conductor thickness and shape.

Another problem in device simulation is the definition of a set of linear independent currents for inductances matrix extraction. We solve this problem in close connection with equivalent circuit representation of the physical device [20]. We consider so-called fundamental loops in the circuit. Any other loop within the circuit can be presented as the unification of fundamental loops. Each loop uniquely defines the current path and the sequence of terminals in the layout. Also, each loop defines the sequence of oriented inductances in the equivalent circuit. The program 3D-MLSI calculates a physical inductance matrix for the currents in fundamental loops. Then it is possible to set equal schematic and physical fluxoids in fundamental loops and to calculate the values of inductances in the equivalent circuit. We realized the schematic inductance calculation algorithm in the limits of the analytical calculations program MAPLE. The details of this technique will be published elsewhere.

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